Numerical TRL Calibration Technique For Parameter Extraction of Planar Integrated Discontinuities in a Deterministic MoM Algorithm

Lin Li, Ke Wu, *Fellow, IEEE*, and Lei Zhu, *Senior Member, IEEE*

***Abstract*—In this letter, a thru-reflect-line (TRL) calibration procedure is applied and integrated with a full-wave method-of-moments (MoM) simulator for the parameter extraction of planar discontinuities and circuits. Three TRL calibration standards are numerically formulated and consistently characterized by the MoM simulator. An equivalent circuit model of a circuit discontinuity of interest can then be extracted by calibrating out the erroneous effect of port discontinuity in the deterministic MoM algorithm. As an example, a microstrip open-end circuit is comparatively studied in terms of its equivalent fringing capacitance, and effectiveness of the proposed technique is verified.**

***Index Terms*—Equivalent circuit model, full-wave method-of-moments (MoM) simulator, planar discontinuity and circuit, thru-reflect-line (TRL) calibration technique.**

I. Introduction

A NUMBER of commercial method-of-moments (MoM) simulators[1] have successfully been developed that allow one to implement accurate full-wave simulation and optimization of planar integrated circuits and antennas. To meet the ever-stringent efficient requirement in designing an electrically large planar structure, it is always preferable in practice to segment the overall complex geometrical layout into a number of electrically small discontinuity elements and then carry out a synthesis and optimization procedure based on its circuit network linked topology. Following our previous work [1], with our developed admittance-type MoM package, it has been demonstrated that the excited port field in such a deterministic scheme leads to the emergence of a so-called "port discontinuity" [2], and this unwanted effect brings up a very adverse impact on the directly de-embedded circuit parameters. To solve this problem, a numerical calibration technique, namely, short-open calibration (SOC) [1], was originated and developed in our MoM algorithm to remove this error term related to the port discontinuities, as well as other inherent numerical noises, so that we can accurately extract the core equivalent circuit model of interest.

Considering that every commercial MoM simulator can only provide the calculated network parameters at a specified external location along the feeding line, our SOC technique was found difficult in theory for its compatibility and integration with them. It is well known that the thru-reflect-line (TRL) calibration technique [3] has been widely used in microwave measurements, and it was also deployed in [4] to extract numerically the S-parameters of planar circuits from full-wave MoM simulations. In this letter, this TRL is applied to integrate itself with a deterministic MoM commercial simulator for the parameter extraction of planar discontinuities so that their equivalent circuit models can be obtained. To begin with, the numerical TRL scheme is briefly described, and a simple microstrip open-end circuit is then used as an example to investigate the derived open-end fringing capacitance with and without the use of the TRL technique. Results of other techniquess, including those of closed-form equations, are also compared.

II. Numerical TRL Technique

Fig. 1(a) illustrates the geometry of a two-port microstrip discontinuity under modeling, comprising one core discontinuity block and two feeding line blocks. At first, the S-matrix parameters at the two external ports can be easily obtained by using numerical simulations with one of the commercial MoM simulators. In our investigation, the IE3D package of Zeland, Inc., was used. To simplify the analysis, one usually converts such an S-matrix into its corresponding wave cascading matrix $[T_{EXT}]$. Following a standard TRL procedure [3], the discontinuity and two feeding line blocks in Fig. 1(a) are then considered as the device under test (DUT) and two error boxes as depicted in Fig. 1(b). In Fig. 1(b), the terms $[T_A]$, $[T_B]$, and $[T_{DUT}]$ stand for the wave cascading matrices of two error boxes and the DUT box, respectively. In order to evaluate and calibrate out these two error boxes, three TRL calibration standards, i.e., thru reflect and line connections, are defined in the format of equivalent network topology, as shown in Fig. 1(c)–(e).

Through the numerical implementation of these standards with the MoM simulator, one can immediately derive the S-matrices for the two-ports thru and line connections as well as reflection coefficients for the one-port reflect connection, namely, S_{11R} and S_{22R}. Furthermore, one can convert the first two S-matrices into their related cascading matrices $[T_T]$ and $[T_L]$. On the basis of cascaded network topologies, as shown

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L. Li and K. Wu are with the Poly-Grames Research Center, Department of Electrical Engineering, Ecole Polytechnique de Montreal, Montreal, QC H3C 3A7 Canada (e-mail: wuke@grmes.polymtl.ca).

L. Zhu is with the School of Electrical and Electronic Engineering, Nanyang Technological University, Singapore.

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[1]Commercial MoM simulators: *Agilent Momentum, Ansoft Ensemble, Sonnet EM Suite, Jansen LINMIC+/N, Zeland IE3D*, etc.

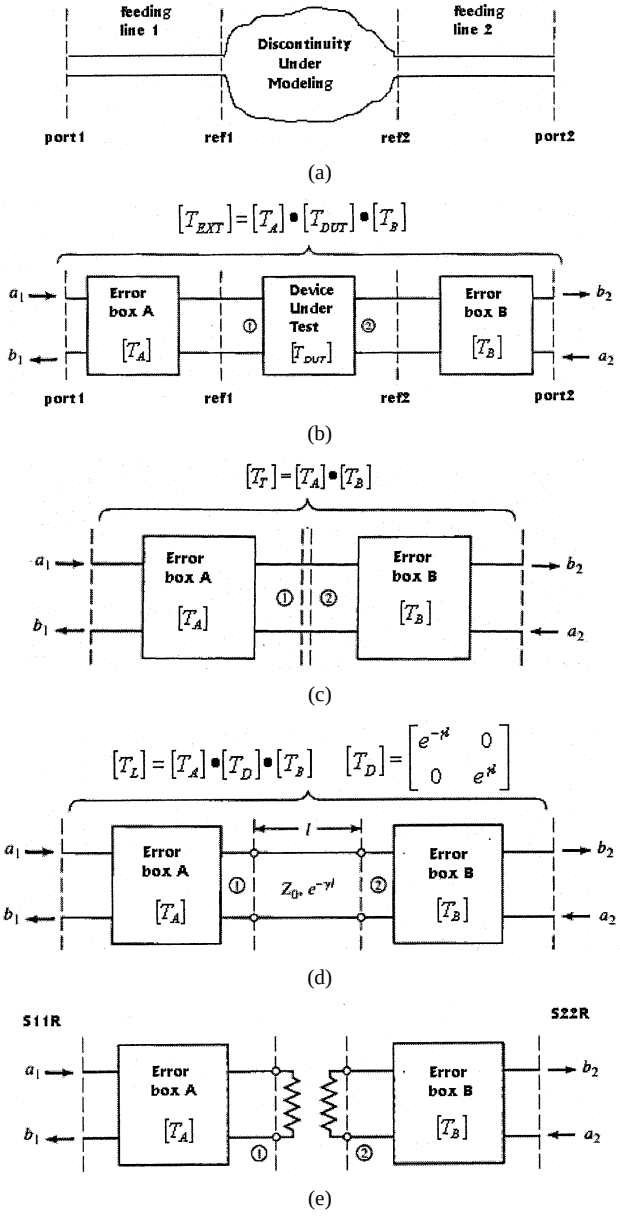

Fig. 1. Block diagram of the numerical TRL calibration procedure. (a) Two-port circuit discontinuity under modeling. (b) Two-port equivalent device under test (DUT). (c) Thru connection. (d) Line connection. (e) Reflect connection.

in Fig. 1(c)–(e), all the parameters of two error boxes $[T_A]$ and $[T_B]$ can analytically be deduced and characterized in terms of those of the above-obtained $[T_T]$ and $[T_L]$, as well as the parameters S_{11R} and S_{22R}. In this work, the microstrip open-end circuit is selected as a reflect element due to its high reflection and also its easy formulation in the MoM simulator. Although this is not an ideal reflect standard due to its fringing effect (which will be extracted in the next section), no strict requirement is needed to know the exact reflection coefficient for this nonideal open circuit in the resulting error boxes $[T_A]$ and $[T_B]$ as in [3]. After the matrices $[T_A]$, $[T_B]$, and $[T_{EXT}]$ are known, one can easily derive the DUT matrix $[T_{DUT}]$ with the following equation:

$$[T_{DUT}] = [T_A]^{-1}[T_{EXT}][T_B]^{-1}. \quad (1)$$

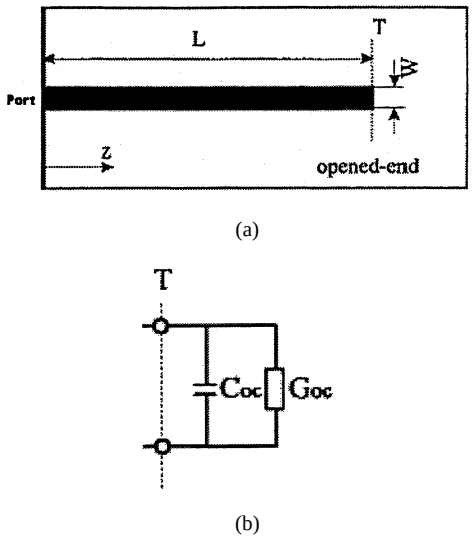

Fig. 2. Geometry and generalized equivalent circuit model of a microstrip open-end circuit. (a) Physical layout. (b) Open-end shunt admittance model.

Note that the frequency limitation of the numerical TRL technique is basically governed by the following two aspects, as discussed in [3], i.e., execution of the software package in question and definition of the TRL standards themselves. To achieve better accuracy, the thru standard should be selected less than 1/4 wavelength while the line standard should be less than 1/2 wavelength at the highest frequency of interested range. Moreover, the electrical length difference between the two standards is required to be discernible, i.e., greater than 20°, at the lowest frequency.

III. Extracted Microstrip Open-End Capacitance

A simple microstrip open-end circuit is now considered as an example to demonstrate the extracted circuit model parameters of a planar circuit on the basis of the above-described TRL scheme. Fig. 2(a) depicts the physical layout arranged for the TRL-based de-embedding of equivalent open-end capacitance (Coc), as shown in Fig. 2(b), in which the radiation-related conductance (Goc) is negligible at low frequency. In our IE3D simulations, a local port model is selected instead of other port models for the deterministic or direct MoM algorithm as detailed in [1]. Therefore, network parameters at the port can directly be derived from the calculated port quantities such as port voltages/currents or amplitudes of incident/reflected waves, without resorting to any additional simulation of current density distributions along the feeding line in the indirect MoM algorithm as in [1].

First, the complex reflection coefficient at the port can numerically be calculated and then converted to its corresponding input admittance with the help of characteristic impedance. Next, the network parameters of the error term with regard to the feed line section [port-to-end section in Fig. 2(a)] can be obtained upon the simulation of three calibration standards as described above. As a result, the load admittance at the open-end can be derived in an analytical way by removing the error box. For the purpose of comparison, such a capacitance is also extracted from the calculated port admittance using a

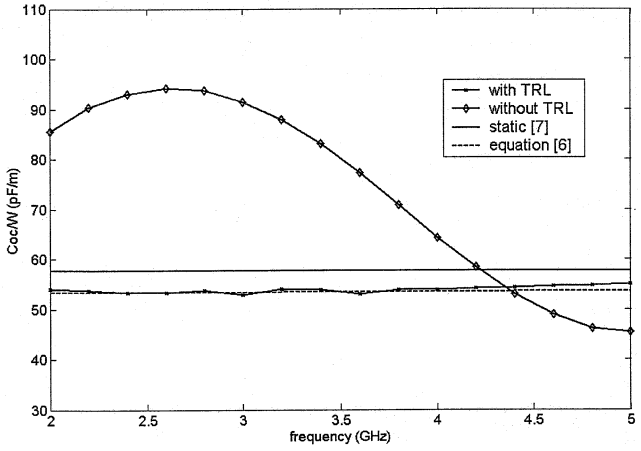

Fig. 3. TRL-extracted open-end fringing capacitance together with those obtained from the non-TRL parameter extraction scheme and two closed-form design equations ($w = h = 0.635$ mm, $\varepsilon_r = 9.9$, $L = 10.4$ mm).

simple transmission line theorem. Fig. 3 shows the obtained normalized capacitance (Coc) using the above two de-embedding techniques against those obtained from closed-form equations as given in [5], [6]. It can be seen that the TRL results appear almost unchanged with frequency and are in a very good agreement with those from formula [5], [6] while the conventional non-TRL results irregularly go up and then fall down as frequency increases. In this case, the unwanted parasitic effects in connection with the port discontinuity are a primordial factor as discussed in [1] and [2].

IV. Conclusion

We have extended the usually measurements-oriented TRL calibration technique to the numerical de-embedding of equivalent circuit models for planar integrated circuits and discontinuities on the basis of full-wave MoM simulations. Our comparative investigation has demonstrated that the proposed numerical TRL scheme is able to calibrate the port discontinuity involved in the deterministic MoM algorithm by formulating three calibration standards. With its easy implementation and direct compatibility in the existing MoM commercial packages, this developed TRL technique has a great potential for accurate CAD and optimization with the extracted circuit models.

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